METHOD AND STRUCTURE IMPROVING ISOLATION BETWEEN MEMORY CELL PASSING GATE AND CAPACITOR

ABSTRACT

[0036] A memory cell comprising a capacitor having a dielectric layer interposing first and second vertically disposed electrodes, an insulating lining located over the capacitor, and a transistor gate extension passing over the capacitor. A spacer isolates an end of one of the capacitor electrodes from the transistor gate extension. In one embodiment, the spacer includes a first non-planar profile configured to engage a second non-planar profile comprising ends of the one of the capacitor electrodes and the insulating lining.